What is claimed is:

1. A mask read only memory comprising:

a semiconductor substrate;

a plurality of buried impurity diffusion regions formed in the semiconductor substrate and near the surface of the semiconductor substrate, each of the plurality of buried impurity diffusion regions being parallel to each other, being separated from each other by a first predetermined interval, and extending in the same direction;

a plurality of word lines formed over the semiconductor substrate, the word lines being to each other, being separated from each other by a second predetermined interval, and extending in a direction perpendicular to the direction that the buried impurity diffusion regions extend;

a gate insulation layer formed between the semiconductor substrate and the plurality of word lines;

a plurality of channel regions defined by the areas between the buried impurity diffusion regions that are overlapped by the word lines; and

a plurality of pad conductive layers formed in the channel regions, the pad conductive layers forming an ohmic contact with the word lines.

2. A mask read only memory, as recited in claim 1,

wherein the plurality of buried impurity diffusion regions act as bit lines and as sources/drains of cell transistors, and

wherein the word lines act as gate electrodes of the cell transistors.

3. A mask read only memory, as recited in claim 1, wherein the pad conductive layers are formed to have an island shape in the channel regions.

4. A mask read only memory, as recited in claim 1,

wherein the word lines comprise a polycide layer in which a polysilicon layer and a metal silicide layer are stacked, and

wherein the pad conductive layers comprise polysilicon.

5. A mask read only memory, as recited in claim 1, wherein the pad conductive layers are formed to a thickness of about 300-1000 Å.

6. A mask read only memory, as recited in claim 1, further comprising grown insulation layers formed over the surface of the buried impurity diffusion regions.

7. A mask read only memory, as recited in claim 6, wherein the grown insulation layers have a thickness of about 100-1000 Å.

8. A mask read only memory, as recited in claim 6, wherein the grown insulation layers have horn portions at their edges.

9. A mask read only memory, as recited in claim 1, wherein the buried impurity diffusion regions are formed to have a double diffusion drain (DDD) structure in which high-concentration buried impurity diffusion regions are surrounded by low-concentration buried impurity diffusion regions.

10. A mask read only memory, as recited in claim 1, further comprising a plurality of cell isolation impurity layers formed in regions between the buried impurity diffusion regions that are not overlapped by the pad conductive layers.

11. A method of fabricating a mask read only memory, comprising:

forming a gate insulation layer over a semiconductor substrate;

forming a plurality of conductive layer patterns over the gate insulation layer, the conductive layer patterns being formed in parallel, being separated from each other by a first predetermined interval, and extending in the same direction;

performing ion implantation, using the conductive layer patterns as a mask, to form buried impurity diffusion regions in an exposed region of the semiconductor substrate between the conductive layer patterns;

forming a conductive layer over the conductive layer patterns and the buried impurity diffusion regions; and

etching the conductive layer and the conductive layer patterns to form a plurality of word lines and a plurality of pad conductive layers,

wherein the word lines are formed in parallel, are separated from each other by a predetermined interval, and extend in a direction perpendicular to the buried impurity diffusion regions,

wherein channel regions are defined by the areas between the buried impurity diffusion regions that are overlapped by the word lines, and

wherein the pad conductive layers are formed to have an island shape in the channel regions, and form ohmic contacts with the word lines.

12. A method of fabricating a mask read only memory, as recited in claim 11, wherein the forming of the buried impurity diffusion regions comprises:

implanting impurity ions at a low concentration into semiconductor substrate using the conductive layer patterns as a mask, to form low-concentration buried impurity diffusion regions that are self-aligned with the conductive layer patterns;

simultaneously forming spacers on the sidewalls of the conductive layer patterns and removing exposed portions of the gate insulation layer, so as to partially expose the low-concentration buried impurity diffusion regions; and

implanting impurity ions at a high concentration into semiconductor substrate, using the conductive layer patterns and the spacers as a mask, to form high-concentration

buried impurity diffusion regions in the low-concentration buried impurity diffusion regions.

13. A method of fabricating a mask read only memory, as recited in claim 12, wherein in the high-concentration impurity implantation, arsenic (As) ions are implanted at an energy of about 40 keV to a dose of about 5.0×10^{15} ions/cm^2.

14. A method of fabricating a mask read only memory, as recited in claim 12, further comprising oxidizing the exposed surface of the semiconductor substrate to form grown insulation layers over the surface of the high-concentration buried impurity diffusion regions.

15. A method of fabricating a mask read only memory, as recited in claim 14, wherein the grown insulation layers are formed to a thickness of about 100-1000 Å.

16. A method of fabricating a mask read only memory, as recited in claim 11, wherein the forming of the conductive layer patterns comprises:

forming a conductive material layer over the gate insulation layer;

forming an etch mask layer on the conductive material layer;

forming spacers on the sidewalls of the etching mask layer; and

etching the conductive material layer using the etching mask layer and the spacers as an etching mask to form the conductive layer patterns,

wherein the forming of the buried impurity diffusion regions comprises implanting impurities over the entire surface of the resultant structure using the etch mask layer a, the spacers, and the conductive layer patterns as a mask, to form buried impurity diffusion regions in an exposed region of the semiconductor substrate.

17. A method of fabricating a mask read only memory, as recited in claim 16, further comprising, after the forming of the buried impurity diffusion regions, oxidizing the exposed surface of the semiconductor substrate to form grown insulation layers over the surface of the buried impurity diffusion regions.

18. A method of fabricating a mask read only memory, as recited in claim 17, wherein the grown insulation layers are formed to have a thickness of about 100-1000 Å.

19. A method of fabricating a mask read only memory, as recited in claim 11, wherein the pad conductive layers comprise a material capable of forming the ohmic contacts with the word lines.

20. A method of fabricating a mask read only memory, as recited in claim 19, wherein the pad conductive layers comprise polysilicon, and the word lines comprise a polycide layer in which a polysilicon layer and a metal silicide layer are stacked.

21. A method of fabricating a mask read only memory, comprising:

forming a gate insulation layer over a semiconductor substrate;

forming a first polysilicon layer over the gate insulation layer;

forming photoresist patterns over the first polysilicon layer, which entirely cover a peripheral circuit region but are patterned in a cell array region to expose regions that are to become buried impurity diffusion regions;

performing ion implantation using the photoresist patterns as a mask to form a plurality of buried impurity diffusion regions near the surface of the semiconductor substrate, wherein the buried impurity diffusion regions are formed in parallel, are separated from each other by a first predetermined interval, and extend in the same direction;

removing the photoresist patterns, and sequentially stacking a second silicon layer and a metal silicide layer over the first polysilicon layer; and

sequentially etching the first and second polysilicon layers and the metal silicide layer so as to form a plurality of word lines, wherein the word lines are formed in parallel, are separated from each other by a second predetermined interval, and extend in a direction perpendicular to that of the buried impurity diffusion regions.

22. A method of fabricating a mask read only memory, as recited in claim 21, wherein the buried impurity diffusion regions act as bit lines and as sources/drains of cell transistors.

23. A method of fabricating a mask read only memory, as recited in claim 21, further comprising doping first and second polysilicon layers with $POCl_3$ ions so as to provide conductivity to the first and second polysilicon layers.

24. A method of fabricating a mask read only memory, as recited in claim 21, wherein the gate insulation layer is formed to a thickness of about 50-150 Å, the first polysilicon layer is formed to a thickness of about 100-1000 Å, the second polysilicon layer is formed to a thickness of about 500-1500 Å, and the metal silicide layer is formed to a thickness of about 500-2000 Å.